What is claimed is:

1. A method for crystallizing an amorphous film into large grains comprising the steps of:

a) depositing a layer of the amorphous first film;

b) doping the amorphous first film with a first concentration of transition metal, to form a first density of transition metal nucleus sites, with the nucleation sites being separated by a first distance, whereby a low density of nucleation sites is formed; and

c) annealing to form a first area of a single grain of crystallized first film, whereby a crystallized film is prepared for the fabrication of a single crystal transistor.

2. A method as in claim 1 including a further step, following Step c), of:

d) removing transition metal semiconductor compound surrounding the first area of crystallized first film, whereby the film is cleaned of materials which promote high leakage currents.

3. A method as in claim 1 in which Step b) includes using an ion implantation method to dope amorphous first film with transition metal within a rectangular window having a width in the range from 20 to 50 microns.

4. A method as in claim 1 in which Step b) includes using an ion implantation method to dope amorphous first film with transition metal within a rectangular window having a length in the range from 60 to 150 microns.

5. A method as in claim 3 in which Step b) includes using an ion implantation method to dope amorphous first film with transition metal within a rectangular window having a width in the range from 20 to 50 microns and a length of 50 microns, or greater, and in which Step c) includes forming at least a second area of a single grain crystallized first film.

6. A method as in claim 1 in which Step b) is performed, at least partially, simultaneously with Step c), whereby transition metal is continually introduced during the annealing process to support the lateral growth of crystallization.

7. A method as in claim 6 including further steps, following Step a), of:

a_1) depositing an insulator film having a first thickness overlying the amorphous first film;

a_2) depositing the transition metal overlying the insulator film first thickness to form a window of transition metal; and

in which Step c) includes the diffusion of transition metal through the insulator film first thickness into the amorphous first film, whereby the density of transition metal nucleuses is controlled.

8. A method as in claim 7 in which Step a_2) includes selectively etching the transition metal deposited in Step a_2) to form a window of transition metal, whereby the size of the first area of crystallized film is influenced.

9. A method as in claim 7 in which Step a_1) includes depositing the insulator film with an initial thickness, in which the insulator film is selectively etched to form an area having a first thickness, less than the initial thickness, and in which Step a_2) includes forming a window of transition metal over the insulator film first thickness, whereby the size of the first area of crystallized film is influenced.

10. A method as in claim 7 in which the ratio of the area of the transition metal window of Step a_2), to the first area of crystallized film is in the range from 1:1 to 1:3.

11. A method as in claim 10 in which Step c) includes the first area of crystallized first film being in the range from 20 to 8,000 square microns (μ^2).

12. A method as in claim 7 in which Step a_2) includes the transition metal window being a rectangle having a width in the range from 20 to 50 microns.

13. A method as in claim 7 in which Step a_2) includes the transition metal window being a rectangle having a length in the range from 60 to 150 microns.

14. A method as in claim 7 in which Step a_2) includes the transition metal window being a rectangle having a width in the range

from 20 to 50 microns and a length of 50 microns, or greater, and in which Step c) includes forming at least a second area of crystallized first film.

15. A method as in claim 9 in which Step a_1) includes depositing an insulator layer having an initial thickness of 500 Å, or greater.

16. A method as in claim 7 in which Step a_1) includes an insulator first thickness in the range from 10 to 100 Å.

17. A method as in claim 7 in which Step a_1) includes an insulator material selected from the group consisting of silicon dioxide and silicon nitride.

18. A method as in claim 7 in which Step a_2) includes depositing transition metal having a thickness in the range from 10 to 1000 Å.

19. A method as in claim 1 in which Step b) includes the first concentration of transition metal being no more than 2×10^{19} atoms per cubed centimeter.

20. A method as in claim 1 in which Step b) includes the first density of transition metal nucleus sites being no more than 1×10^{7} square centimeters.

21. A method as in claim 1 in which Step b) includes a first distance between transition metal nucleus sites of no less than 2 microns.

22. A method as in claim 1 in which Step b) includes depositing a transition metal selected from the group consisting of Al, Ni, Ti, Co, and Pd.

23. A method as in claim 1 including further steps, preceding Step c), of:

b_1) ramping the temperature up to the annealing temperature of Step c) at a rate greater than 5 degrees C per second, whereby the first film is annealed at the intended temperature of Step c) for a larger crystal grain.

24. A method as in claim 1 in which Step c) includes using a Rapid Thermal Annealing (RTA) process at a temperature in the range from 600 to 800 degrees C, and a time duration in the range from 1 second to 15 minutes.

25. A method as in claim 24 in which Step c) includes using a Rapid Thermal Annealing (RTA) process at a temperature in the range from 700 to 750 degrees C, and a time duration in the range from 1 to 5 minutes.

26. A method as in claim 25 in which Step c) includes using a Rapid Thermal Annealing (RTA) process at a temperature of

approximately 720 degrees C and a time duration of approximately 2 minutes.

27. A method as in claim 1 wherein a glass substrate is provided, and in which Step a) includes depositing the first film overlying the glass substrate.

28. A method as in claim 1 including the further steps of:

e) forming transistor source, drain, and channel regions within the first area of crystallized film, whereby the source, drain, and channel regions are formed from a single crystal grain, without the presence of transition metal semiconductor compounds;

f) forming a gate oxide layer;

g) forming a gate electrode;

h) implanting doping species; and

i) annealing to activate the implanted species, whereby both top gate and bottom gate TFTs are formed.

29. A method as in claim 1 in which Step a) includes an amorphous first film selected from the group consisting of silicon, germanium, silicon carbide, and silicon-germanium compounds.

30. A method as in claim 1 in which Step a) includes an amorphous first film having a thickness in the range from 200 to 10,000 Å.

31. A method of annealing a semiconductor film with a transition metal to form a crystallized film with large crystal grains, the method comprising the steps of:

a) heating the semiconductor film to a temperature in the range from 700 to 750 degrees C;

b) heating the semiconductor film for a duration in the range from 1 to 5 minutes;

c) supplying a transition metal concentration of no more than 2×10^{19} atoms/cm^3;

d) maintaining a transition metal nucleation site density of no more than 1×10^7/cm^2;

e) maintaining a distance between transition metal nucleation sites of no less than 2 microns; and

f) forming large grains of crystallized semiconductor film corresponding to the distance between transition metal nucleation sites.

32. A first thin-film transistor (TFT) comprising source/drain and channel regions of a single grain of crystallized first film material formed from doping an amorphous first film with a transition metal through a transition metal window at a first concentration, first density of nucleation sites, and a first distance between nucleation sites, annealing said amorphous first film to form a first area of crystallized first film which is a single grain of crystal, and etching a pattern in said first area of crystallized first film to form the source/drain regions, whereby a transistor is formed having high electron mobility and low leakage current in the transistor active areas.

33. A TFT as in claim 32 further comprising:

a gate electrode;

a gate oxide layer overlying said gate electrode; and

in which said gate electrode and gate oxide layer are deposited before said first film, whereby a bottom gate TFT is fabricated.

34. A TFT as in claim 32 further comprising:

a gate oxide layer overlying said channel region; and

a gate electrode overlying said gate oxide layer, whereby a top gate TFT is fabricated.

35. A TFT as in claim 32 in which said first film material is selected from the group consisting of silicon, germanium, silicon carbide, and silicon-germanium compounds.

36. A TFT as in claim 32 in which the transition metal is selected from the group consisting of Al, Ni, Ti, Co, and Pd.

37. A TFT as in claim 32 in which the temperature is ramped-up to the annealing temperature at a rate greater than 5 degrees C per second, whereby the first film is annealed at the intended temperature for larger crystal grains.

38. A TFT as in claim 32 in which the annealing is performed with an RTA process at a temperature in the range from 600 to 800 degrees C, for a time duration in the range from 1 second to 15 minutes.

39. A TFT as in claim 38 in which the annealing is performed with an RTA process at a temperature in the range from 700 to 750 degrees C, for a time duration in the range from 1 to 5 minutes.

40. A TFT as in claim 39 in which the annealing is performed with an RTA process at a temperature at approximately 720 degrees C and a time duration of approximately 2 minutes.

41. A TFT as in claim 32 in which transition metal semiconductor compound surrounding said first area of crystallized first film is removed when said source/drain regions are defined, whereby said crystallized film is cleaned of materials which promote high leakage currents.

42. A TFT as in claim 32 in which said transition metal is doped within a rectangular window overlying said first area of crystallized film, having a width in the range from 20 to 50 microns.

43. A TFT as in claim 32 in which said transition metal is doped within a rectangular window overlying said first area of crystallized film, having a length in the range from 60 to 150 microns.

44. A TFT as in claim 32 wherein at least a second TFT is formed adjoining the first TFT, in which at least a second area of crystallized first film is formed adjoining said first area of crystallized first film, and in which said transition metal is doped within a rectangular

window overlying said first and second areas of crystallized film having a width in the range from 20 to 50 microns and a length of 50 microns, or greater.

45. A TFT as in claim 32 in which said amorphous first film is doped with said transition metal to said first concentration of transition metal less than 2×10^{19} atoms per cubed centimeter.

46. A TFT as in claim 32 in which said amorphous first film is doped with said transition metal to said first density of transition metal nucleus sites is less than 1×10^{7} square centimeters.

47. A TFT as in claim 32 in which the first distance between said transition metal nucleus sites is no less than 2 microns.

48. A TFT as in claim 32 in which the ratio of said transition metal window area to said first area of crystallized film is in the range from 1:1 to 1:3.

49. A TFT as in claim 32 in which said first area of crystallized first film is in the range from 20 to 8,000 square microns (μ^2).

50. A TFT as in claim 32 in which transition metal doping is selected from the group consisting of ion implantation and CVD deposition.

51. A TFT as in claim 32 in which said transition metal doping occurs, at least partially, simultaneously with the annealing of said first film, whereby said transition metal is continually introduced during the annealing process to support the lateral growth of crystallization.

52. A TFT as in claim 51 in which an insulator film having a first thickness is deposited over said amorphous first film, with said transition metal being deposited overlying said insulator film, and in which said transition metal diffuses through said insulator film into said amorphous first film first thickness during annealing, whereby the formation of said transition metal nucleuses is controlled.

53. A TFT as in claim 52 in which said transition metal overlying said insulator film is selectively etched before annealing to form said transition metal window, whereby the size of said first area of crystallized first film is influenced.

54. A TFT as in claim 52 in which said insulator film is deposited with an initial thickness and selectively etched to form an area having a first thickness, less than the initial thickness, and in which said transition metal is deposited over said first thickness of insulator film to form said transition metal window, whereby the size of said first area of crystallized film is influenced.

55. A TFT as in claim 54 in which said initial thickness is 500 Å, or greater.

56. A TFT as in claim 52 in which said insulator film has a first thickness in the range from 10 to 100 Å.

57. A TFT as in claim 52 in which said insulator material is selected from the group consisting of silicon dioxide and silicon nitride.

58. A TFT as in claim 52 in which said transition metal is deposited with a thickness in the range from 10 to 1000 Å.

59. A TFT as in claim 32 further comprising a glass substrate, and in which said crystallized first film is formed overlying said glass substrate.

60. A TFT as in claim 32 in which said amorphous first film has a thickness in the range from 200 to 10,000 Å.